DRIVER FOR PHASE SHIFT KEYING MODULATOR USING A MULTILEVEL MMIC TECHNOLOGY FOR K-BAND SPACE APPLICATIONS

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ABSTRACT

This paper presents a new simple design of an integrated driver using a multilevel MMIC technology that can be used to operate a NRZ (No Return to Zero of digits) two, four or eight phase shift keying direct modulator. It can be fed by any digital signals featuring any low level ($V_{Output\ Low}$) between 0 V and 0.5 V and an high level ($V_{Output\ High}$) between 2.5 V and 8 V. It therefore provides a full compatibility with most usual logic families. An MMIC featuring a K-band (17.5 to 21.5 GHz) Bi-Phase Shift Keying modulator (BPSK) along with the proposed driver has been designed. The measured performances are : 6° maximum phase error and 1.1 dB maximum amplitude error over the full 4 GHz bandwidth.

INTRODUCTION

The arrival of MMICs has resulted in a major improvement towards the active microwave circuits miniaturization. Today, the last developments in MMIC processing techniques and in Computer-Aided Design (CAD) make it possible to consider the integration on a same chip of both microwave and conventional (digital or analog) circuits.
The full integration of a K-band phase shift keying modulator along with its driver showing a full compatibility with most usual digital signals illustrates this new approach in terms of circuit simplification and higher integration.
This driver has been manufactured in the ED02AH process (technology Pseudomorphic High Electron Mobility Transistor 0,2 µm, multilevel : normally-off V_t = 0,1 V, normally-on V_t = -0,9 V) of Philips Microwave Limeil foundry. The measurements are presented in this paper.

I. DRIVER PRINCIPLE

The driver provides an appropriate interface between the logic circuit supplying the digitized data and the switching PHEMT transistors of the modulator. The circuit innovation resides in the use of a multilevel technology. This one makes it possible to feed directly the normally-off switching transistor (positive threshold voltage) with a positive voltage supplied for example by CMOS or TTL logic circuits whatever is the V_{OH} voltage value (between 2.5 and 8 V).
The circuit driver must be able to supply the two control states of the modulator normally-off transistors which are:

state ON : $V_g = 0.5$ V
state OFF : $V_g = 0$ V ($< V_t = 0.1$ V).

And also, it must be compatible with logic signals having a voltage V which checks the following conditions :
- for a TTL logic gate :

$V = V_{OL\ max\ TTL} = 0.5\ V \Rightarrow V_g < 0.1\ V$
$2.5\ V \leq V_{OH\ TTL} \leq 3.4\ V \Rightarrow 0.4 \leq V_g \leq 0.8\ V$

- for a CMOS logic gate :

$V = V_{OL\ min\ CMOS} = 0\ V \Rightarrow V_g < 0.1\ V$

$V = V_{OH\ max\ CMOS} = 5\ V$ (possibility up to 8 V) $\Rightarrow 0.4 \leq V_g \leq 0.8\ V$

($V_g = 0.8$ V gate-source polarisation maximum voltage of normally-off transistor given by the founder).

The characteristic $V_g(V)$ (see Figure 2) summarizes the above statements. We notice that they correspond to a non linear characteristic which forbids the use of resistance bridge. So, we have designed a voltage divider bridge where the first element is a normally-on transistor (see Figure 1) which is a current source for V_{OH} and a resistance for V_{OL}. The current source state limits the control voltage on the modulator normally-off transistor in order to avoid forward biasing the gate. Two resistors, R2 and R3, have been added in order to adjust its characteristics. The resistors constituting the divider bridge have been calculated using the conditions above and also care has been taken to limit the time constants to transmit high data rates.

The simulations done with the Hewlett Packard Libra 6.1 software in DC bias analysis are shown in figure 3 and fit the conditions stated above.

II. BPSK MODULATOR WITH DRIVERS DESIGN

The driver has been integrated with a BPSK modulator whose the working principle is the following :

The BPSK direct modulator provides a modulation of a microwave carrier with two opposite phase states and equal amplitudes. The working principle [1] requires two filters, one high-pass type and the other low-pass type with the 180° transfer phase difference which are switched at the rate of the modulation signal. The biphase modulated signal is formed by the alternative flow of the RF carrier in one of the two filters according to the modulation signal. The high-pass and low-pass filters are composed of two LC cells in lumped elements. The switch is made of two shunt normally-off cold PHEMT transistors, controlled by the gate-source voltage Vg. This circuit doesn't need any DC bias.

Simulations and layout of BPSK modulator with drivers chip :

The operating frequency band for the related application is from 17.5 to 21.5 GHz. Indeed the increase of digital rates for multimedia telecoms and payload telemetry enhances the interest in more and more higher frequencies which allow larger pass-bands, needed for high data rate transmission. The multimedia telecoms satellites like SPACEWAY on Geostationary Earth Orbit or TELEDESIC [2] on Low Earth Orbit, demodulate on board the received signals and after data processing ensure the downlink by direct modulation of a carrier in K-band in 17.5-21.5 GHz frequency range. The BPSK modulator with drivers layout is shown in Figure 4. After the data inputs I and $\bar{I}$, the drivers controlling the modulator transistors are noteworthy. This circuit has been integrated into a chip whose size is 2 x 1.5 mm^2. We have considered the following specifications : phase accuracy between states $\leq \pm 5°$, residual amplitude modulation ≤ 1 dB peak to peak, insertion losses < 5 dB and input and output matchings < -10 dB. The small signal circuit simulations and optimisations have enabled us to guarantee the following performances on a 4 GHz band (20% of frequency bandwidth) : 1.3° maximum phase error , 0.24 dB maximum amplitude error, scattering parameters S11 and S22 < -10 dB and S21 > -3.8 dB (see Figure 5). In figure 6, we can see the voltages waveforms : data input I (250 MHz square wave) and output biphase modulated signal (V_{out}). We note that the BPSK modulator with drivers is able to pass a 500 Mbits/s bit rate.

III. MEASUREMENTS

Driver measurements :

A test cell for the driver has been machined in order to test it without the modulator and thus to be able to validate the topology or to improve the concept at the time of a second possible foundry. In measurements on wafer, we have just checked the DC characteristic $V_g(V)$ of the driver. We can see in Figure 3 the very good agreement between simulation and measurement. The driver will be able to describe the two control states of the modulator as stated in the paragraph I.

BPSK modulator with drivers measurements :

At the reception of the chips, considering the parameter $V_{t\ N\text{-}OFF}$ of the Process Control Monitors, we were fear of the dysfunction of the BPSK modulator with integrated drivers. Indeed, the mean of $V_{t\ N\text{-}OFF}$ observed on the wafer was -0.098 V with a standard deviation of 0.077 V instead of being typically 0.1 V. Thus, the normally-off transistors become normally-on what is a major drawback for the nominal operation of BPSK modulator with drivers. Nevertheless on wafer small signal measurements were performed.The

measurements show (see Figure 5) that the modulation is correctly ensured for a TTL or CMOS modulating signal : 6° maximum phase error , 1.1 dB maximum amplitude error on a 4 GHz band ; on the other hand the scattering parameters S11 and S22 < - 5.5 dB and S21 > -12.5 dB are not in the expected range. It is concluded that the proposed topology is very tolerant and it is anticipated that should the threshold voltage of normally-off transistors be 0.1 V in the next foundry, all the characteristics will be clearly better and mostly the insertion losses and the output matching will be improved.

IV. FUTURE APPLICATIONS

Today, the satellites constellations for the multimedia telecoms and payload telemetry request high bit rates from one Gbits/s to two Gbits/s. The BPSK modulator is limited for these high bit rate applications. Therefore we must use modulations with a better spectral efficiency, as the four and eight phase shift keying modulations which have 2 bits/s/Hz and 3 bits/s/Hz spectral efficiency respectively. These QPSK and 8PSK modulators have been manufactured in the same foundry that the BPSK modulator with drivers. The distributed 8PSK modulator calls for a new concept which has been the subject of a patent [5]. It consists of four identical BPSK modulators fed successively by signals out of phase of 45° and combined in phase by Wilkinson couplers. This phase displacement is achieved by a input circuit, based on a non uniform transmission line made of a succession of LC cells similar to the one used in distributed amplifiers. This modulator which has been integrated into a chip whose size is 3 x 3 mm^2, presents encouraging performances : 15° maximum phase error, 2 dB maximum amplitude error on a 4 GHz band. We notice also that the distributed 8PSK modulator is more sensitive to phase defects between states, but this can be solved by demodulation algorithms and error codings more efficient like the trellis coding. This modulator will be shortly integrated with drivers and could transmit high wished data rates.

CONCLUSION

The proposed design demonstrates the feasability of an interface between an analog BPSK modulator and a logic circuit supplying the digitized data. This new generation of multifunctions MMIC chips reduces the number of circuits and simplifies the system design. The next step will be an improved the design of the driver for high bit rates up to one Gbits/s or more. Also, the driver should be able to operate with four and eight phase shift keying modulators already realized in the same foundry and which take advantage on having a more narrow spectrum occupation at equal bit rate.

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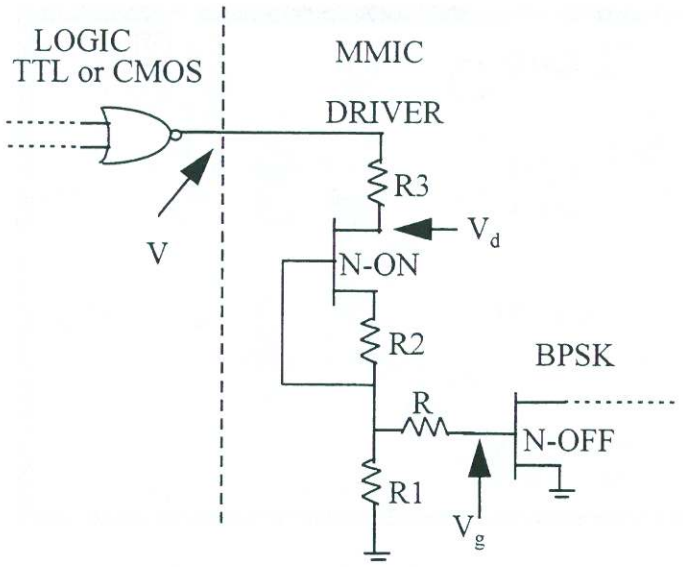

Figure 1 : Schematic of the MMIC driver

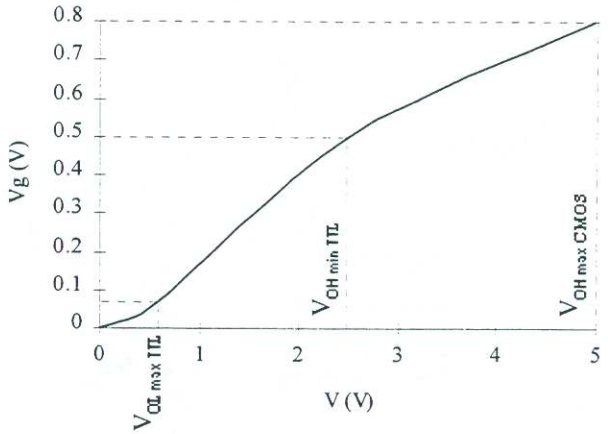

Figure 2 : Theoretical $V_g(V)$ characteristic for the driver that must handle TTL and CMOS logic levels

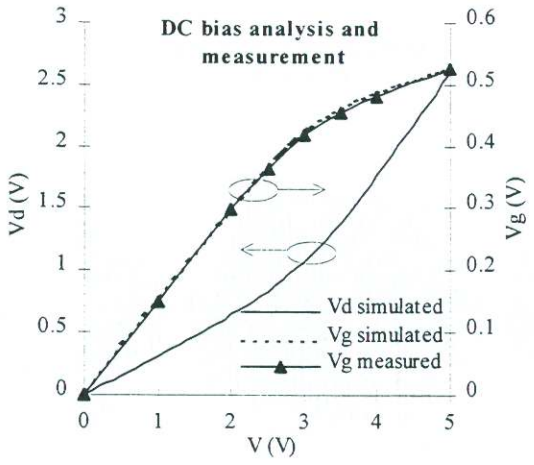

Figure 3 : Measured and simulated $V_g(V)$ characteristic of the implemented driver - Vd(V) is also given (PHEMT N-ON)

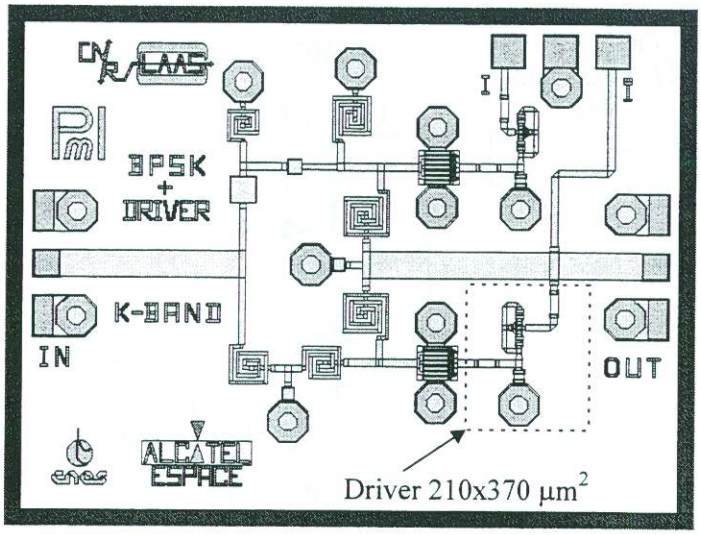

Figure 4 : Layout of the BPSK modulator with drivers (2x1.5 mm^2)

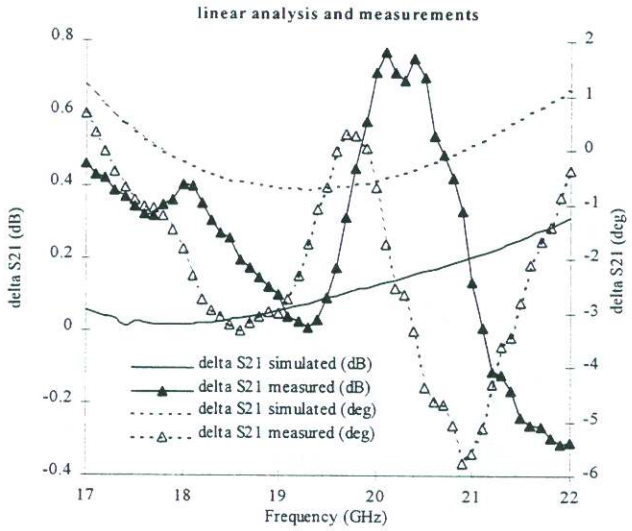

Figure 5 : Amplitude and phase errors of BPSK modulator with drivers

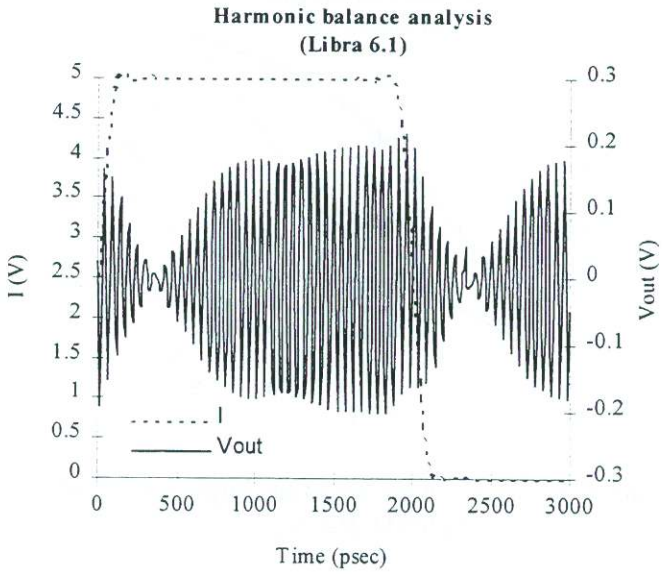

Figure 6 : Waveforms of signals I and V_{out}